IN THE CLAIMS

Please amend claims 1-10, cancel claim 11, and add new claims 12 and 13.

Claim 1. (Currently amended) A system for addressing a data storage unit used in at least one of server and client computers, which comprises:

means for converting a format of data on an external bus ~~into~~ such that the data are accessed on an internal bus for use in the system;

a memory card module connected to the internal bus for storing data on the internal bus ~~therein~~, wherein the memory card module ~~being divided into~~ includes a plurality of memory modules each having a plurality of equally-sized memory blocks; and

means for ~~processing~~ writing data on the internal bus ~~in~~ to the memory module and reading out the data therefrom.

Claim 2. (Currently amended) The system of claim 1, wherein the internal bus is a PCI (Peripheral Component Interconnect ~~Bus~~) interface bus

Claims 3. (Currently amended) The system of claim 1, wherein the ~~converting means includes~~ external bus is a SCSI (Small Computer System Interface) ~~interface~~ bus.

Claim 4. (Currently amended) The system of claim 1, wherein the memory card module is composed of any one of SDRAM(Synchronous Dynamic Random Access Memory), rambus DRAM(Dynamic Random Access Memory), DDR(Double Data Rate) or other equivalent memories.

Claim 5. (Currently amended) The system of claim 1, wherein each of the plurality of equally-sized memory blocks is divided into a predetermined number of equally-sized sub-memories such that the memory module has a hierarchical memory configuration.

Claim 6. (Currently amended) The system of claim ~~1~~ 5, wherein the predetermined number is four.

Claim 7. (Currently amended) The system of claim 5, wherein ~~the memory module employs a tree hierarchical configuration, which again compensates~~ signals inputted to the memory card module of the hierarchical memory configuration are compensated again at ~~an intermediate~~ memory module and memory block stages ~~and forwards it to a lower hierarchy~~.

Claim 8. (Currently amended) The system of claim 7, wherein the memory card module includes a PCI-to-memory controller ~~of a tree hierarchical configuration~~, which is disposed between the internal bus and the ~~plurality of sub-memories~~ memory module as a bridge, for controlling access to the plurality of sub-memories~~, which are distributed in a hierarchical fashion~~.

Claim 9. (Currently amended) The system of claim 8, wherein a clock delay required for compensating the signals in the ~~tree~~ hierarchical memory configuration is ~~designed to allow~~ compensated ~~a clock delay to be compensated~~ at the PCI-to-memory controller.

Claim 10. (Currently amended) The system of claim 4 8, wherein the PCI-to-memory controller activates any of the plurality of sub-memories to be actually accessed and maintains the remaining sub-memories in a low power mode.

Claim 11. (Canceled)

Claim 12. (New) The system of claim 10, wherein the PCI-to-memory controller includes:

a PCI interface controlling unit for performing a standard PCI command, control and data signal processing; and

a plurality of memory controlling units for performing a direct read/write operation for the sub-memories in response to the PCI command from the PCI interface controlling unit.

Claim 13. (New) The system of claim 12, wherein the PCI interface controlling unit includes a register block having a lower address bit, an upper address bit and a select bit, wherein the lower address bit represents addresses included in the range of an address region within a memory map, the upper address represents address set to be used when a memory address region is beyond the address region of the memory map, and the select bit is used to directly access the memory module.